High Performance Demodulator Library

High Performance Demodulator Library for FPGA
Version 1.0

User Manual

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1. High Performance Demodulator Library for FPGA

Single carrier modulations are widely used in modern wireless communication receivers for data transmission and reception. OLYMP Engineering LLC has developed High Performance Demodulator (HPD) Library for FPGA that performs high speed BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM and OQPSK demodulation with symbol rate up to 40 MSPS. The High Performance Demodulator (HPD) Library supports development for FPGA and Windows platforms, which allows developers to analyze, prototype algorithms, and application specific performance on Windows before compiling for FPGA. With LabVIEW and LabVIEW FPGA time to market is reduced drastically and.

The PSK demodulator is mainly used to restore the shifted phases that are modulated at symbol rate to the carrier signals in the transmitter, and reinterpret the phase information back to symbols. The main components included in the HPD Library for FPGA are automatic gain control (AGC), matched filtering, carrier recovery, timing recovery, symbol decision and lock detection. This core can be dynamically programmable for MPSK=2, 4, 8 and 16 or MQAM=8 or 16 or OQPSK demodulation. Once the system locked, both demodulated In-Phase and Quadrature (I/Q) samples and hard-coded symbols are available at the outputs. Figure 1 shows the block diagram of the HPD Library for FPGA. The HPD Library for FPGA processes 16 bit baseband I/Q data. The input data rate requires only 2 times of symbol rate which simplifies requirements for RF part and increases possible maximum symbol rate that can be demodulated. The main data path includes a matched filter using Root Raised Cosine filter (RRC), AGC, Frequency correction, timing recovery, fine tuning/tracking and hard decoding. Following the RRC filter the AGC is used to maximize the dynamic range of the signal magnitude and maintain an optimal output sample level for symbol decision. In the timing loop error detector, Gardner timing recovery technique is provided to achieve a high performance and low SNR recovery. Finally, the symbol decision component encodes the demodulated I/Q samples into 8-bit hard-coded symbols according to user input map table. The lock detector monitors the timing and carrier loop errors and asserts a lock signal when both accumulated errors are within the threshold during a predefined observation time.

The PSK demodulator core processes 16 bit baseband In-Phase (I) and Quadrature (Q) data. The input data rate is required to be 2 times of the symbol rate. The main data path includes a matched filter using Root Raised Cosine filter (RRC), AGC. Matched filter to eliminate inter-symbol interference (ISI). Following the RRC filter the AGC is used to maximize the dynamic range of the signal magnitude and maintain an optimal output sample level for symbol decision. Outputs of the AGC processed by timing error detector Gardner technique based is provided to achieve high performance timing error estimate. Final data after timing error detector is processed by fine tuning to remove residual frequency offset. Finally, the symbol decision component encodes the demodulated I/Q samples into 8-bit hard-coded symbols according to user input mapping table. Both demodulated I/Q samples and hard-coded symbols are available at the outputs.

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The HPD Library is targeted at the NI PXIe-5663, NI PXIe-5665, NI PXIe-7966R, NI PXIe-7971R, NI PXIe-7972R, NI PXIe-7975R and NI PXIe-7976R PXIe modules from National Instruments. The HPD Library is provided as a set of VI's and may be rapidly integrated into your designs with ease of use and detailed help.

AGC and Matched Filtering

The AGC compensates any amplitude loss and maximizes the output dynamic range. It includes a gain error detector and a loop filter that responds to the long-term variation and adjusts the gain for the demodulator. In practical communication systems, pulse shaping is used to effectively compress a transmission bandwidth. One popular pulse shaping technique is to place a root-raised-cosine (RRC) filter in the transmitter and another matched filter in the receiver to create a raised-cosine (RC) filter. The symbol values can be completely recovered without ISI if the data is sampled in the middle of the symbol period.

Timing Recovery, Carrier Recovery and Symbol Decision

The timing recovery is used to build a symbol clock synchronous to the one in the transmitter. The timing recovery loop includes a timing error detector (TED), a loop filter and a timing control unit. Gardner timing error technique is provided as a TED. It uses 2 samples per symbol to generate timing error estimate. This error term is processed by a second order loop filter and is used as the control signals to the timing control unit.

The timing control unit outputs the symbol clock to the estimating function, which calculates actual value from the 2 input samples (provides maximum eye opening). In carrier recovery component, hard decision de-mapping used to remove the residual carrier frequency and recover the phase information. Carrier recovery component includes a phase error detector, and a second order IIR loop filter. The detected phase error is fed back to the phase error detector. Once the residual frequency is locked system, outputs recovered IQ Data.

The input to the symbol decision is 16 bit demodulated I/Q samples from previous step. These samples first of all are converted to polar coordinate representation. An encoder logic encodes the symbols based on the map table. The map table is a 16 bit word array, which allows the user to input their own coding scheme.

Software requirements: LabVIEW (2014 or later), LabVIEW FPGA Module (2014 or later), NI-RIO Device Driver (14.5.0 or later), Modulation Toolkit (4.4 or later), NI-RFSA Driver (14.5 or later).
Hardware requirements: NI PXIe-5663, NI PXIe-5665, NI PXIe-7966R, NI PXIe-7971R, NI PXIe-7972R, NI PXIe-7975R, NI PXIe-7976R.

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2. Software Support

2.1. Software requirements

To installation HPD Library for FPGA toolkit, please take the following steps in order:

Step 1: Download and install VIPM (Virtual Instrument Package Manager >= 2014) software from the link.

Step 2: To install the HPD Library for FPGA toolkit, please go to the website by the following links in the right side of the table and enter the software name of the appropriate file to download. After downloading the files, install them sequentially from I to V . Start each installation process after finishing the previous one (during the installation process follow all the commands).

Software Name	Version
I. LabVIEW 2014	2014 or later
II. LabVIEW FPGA Module	2014 or later
III. NI-RIO Device Driver	14.5.0 or later
IV. Modulation Toolkit	4.4 or later
V. NI RFSA Driver	14.5 or later

Note: If the files indicated in the ''Step 2'' are already installed on the computer, you can install the HPD Library in FPGA toolkit by skipping the ''Step 2''.

To activation the HPD Library for FPGA toolkit product please send your FlexRIO hardware serial number to the E-mail: info@olympmail.am and call Tel.: +374 93 688 597 for more information about activation.

Related Topics:
Hardware requirements

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2.2. Hardware requirements

This table describes the list of hardware needed for the use of the HPD Library for FPGA toolkit. Please go to the website by the following links in the right side of the table to learn more information about the appropriate module for correct use.

Hardware Name	Hardware Type
NI PXIe-5663	Vector Signal Analyzer Module (NI PXIe-5663)
NI PXIe-5665	Vector Signal Analyzer Module (NI PXIe-5665)
NI PXIe-7966R	NI FlexRIO FPGA Module (NI PXIe-7966R)
NI PXIe-7971R	NI FlexRIO FPGA Module (NI PXIe-7971R)
NI PXIe-7972R	NI FlexRIO FPGA Module (NI PXIe-7972R)
NI PXIe-7975R	NI FlexRIO FPGA Module (NI PXIe-7975R)
NI PXIe-7976R	NI FlexRIO FPGA Module (NI PXIe-7976R)

Related Topics:
Software requirements

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3. Activation

E-mail: info@olympmail.am
Tel.: +374 93 688 597
Address: 123 Hovsep Emin EIF Entrance, 102
Yerevan 0051, Armenia

3.1. Software Activation

To get acquainted with the steps of activation of the HPD Library for FPGA toolkit, it is necessary to send us the serial number of NI FlexRIO FPGA Module that you use. After that we will send you a license file for the activation of the HPD Library for FPGA toolkit.

E-mail: info@olympmail.am
Tel.: +374 93 688 597
Address: 123 Hovsep Emin EIF Entrance, 102
Yerevan 0051, Armenia

Related Topics:
Hardware Activation

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3.2. Hardware Activation

It is necessary to send us the Serial Number of NI FlexRIO FPGA Module that you use to activate your HPD Library for FPGA toolkit.

E-mail: info@olympmail.am
Tel.: +374 93 688 597
Address: 123 Hovsep Emin EIF Entrance, 102
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4. Conclusion

OLYMP Engineering LLC has developed a high performance baseband B/Q/8/16PSK, OQPS and 8/16QAM demodulator that works at symbol rate up to 40 MSPS and locks within 30 msec. The HPD Library in FPGA contains all necessary components that are required for demodulation of PSK, QAM waveforms, such as AGC, matched filtering, timing recovery, carrier recovery, symbol decision, and lock detector. The HPD Library for FPGA core can be used to develop a complete solution for communication systems.

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